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**POWER CONVERSION INTEGRATED
CIRCUIT AND METHOD FOR
PROGRAMMING**

BACKGROUND OF THE INVENTION

The present invention relates, in general, to integrated circuits and, more particularly, to a power conversion integrated circuit.

A power supply is controlled to be either on or off by a mechanical switch or a relay. Typically, additional discrete components that are external to the integrated circuit adapt the power supply for use in applications such as cable converters for television sets, computer monitors, video cassette recorders (VCRs), battery chargers for portable communications devices, computer printers, and other electronic systems.

Depending on the particular application, the on/off circuitry of a power supply control circuit includes components such as opto-couplers, latches, resistors, and capacitors. Monolithic circuit integration minimizes the number of components external to the integrated circuit and reduces the cost of power supplies. The number and types of external components along with the cost of the integrated circuit package provide functionality that differentiates among different power supplies. Typically, a switching regulator without on/off circuitry is manufactured in a three pin package. A drawback of these three pin package configurations is that they offer limited functionality within the package.

Accordingly, it would be advantageous to have an inexpensive integrated power supply controller that is capable of operating with many different power supplies. It would be of further advantage for the power supply controller to have a minimal number of discrete external components for controlling the power supply on/off switch circuitry.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a power supply in accordance with an embodiment of the present invention;

FIG. 2 is a schematic diagram of a state circuit for use in the power supply of FIG. 1;

FIG. 3 is a schematic diagram of an interface switch circuit for use with the state circuit of FIG. 1 in accordance with another embodiment of the present invention;

FIG. 4 is a schematic diagram of a microprocessor interface switch circuit for use with the state circuit of FIG. 1 in accordance with yet another embodiment of the present invention; and

FIG. 5 is a schematic diagram of a brown-out interface circuit for use with the state circuit of FIG. 1 in accordance with yet another embodiment of the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

Generally, the present invention provides a circuit with at least four modes of operation for controlling the on/off features of a power supply. By connecting an appropriate interface circuit to a state input pin, the power supply is programmed for specific behaviors when power is applied or when the interface circuitry is activated. Thus, the multifunctionality provided by a state circuit that is integrated with a control circuit is a cost effective solution for controlling the power supply.

FIG. 1 is a block diagram of a power supply 10 in accordance with the present invention. Power supply 10 includes a full-wave bridge rectifier 12, capacitors 14, 24,

and 34, diodes 22 and 32, a transformer 16, a compensated error amplifier 42, and a power converter circuit 44. In particular, full-wave bridge rectifier 12 has a ground connection, a pair of inputs for receiving a line voltage, e.g., 110 volts alternating current (VAC), 220 volts VAC, etc. An output of full-wave bridge rectifier 12 supplies a rectified output signal that is filtered by filter capacitor 14. Filter capacitor 14 has a terminal connected to the output of full-wave bridge rectifier 12 and a terminal connected to a power supply potential such as, for example, ground.

Transformer 16 has a primary side or winding 18 having two terminals, a secondary winding 20 having two terminals, and a secondary winding 30 having two terminals. In particular, one terminal of primary winding 18 is connected to the output of full-wave bridge rectifier 12, and the other terminal of primary winding 18 is connected to a switch output pin 40 of power converter circuit 44.

Secondary winding 20 has a first terminal connected to an anode of a diode 22. A cathode of diode 22 is commonly connected to a first terminal of capacitor 24 and to a terminal 26. The second terminal of capacitor 24 is commonly connected to the second terminal of secondary winding 20 and to a terminal 28. Compensated error amplifier 42 has an input connected to terminal 26, an input connected to terminal 28, and an output connected to feedback pin 46.

Secondary winding **30** has a first terminal connected to an anode of diode **32**. A cathode of diode **32** is commonly connected to a first terminal of capacitor **34** and to a bias pin **36** of power converter circuit **44**. The second terminal of capacitor **34** is commonly connected to the second terminal of secondary winding **30** and to a potential such as, for example, ground.

Power converter circuit 44 is a switched mode power supply integrated circuit or a power conversion integrated circuit having five electrical connection terminals: (1) a bias pin 36, (2) a ground pin 38, (3) a feedback pin 46, (4) a state pin 48, and (5) a switch output pin 40. Power converter circuit 44 is a semiconductor device chip that includes a state circuit 50, a control circuit 52 having an internal regulator, and a transistor 54. State circuit 50 has an input connected to bias pin 36 and another input coupled to state pin 48 of power converter circuit 44. Another input of state circuit 50 is connected to an output of control circuit 52 and receives a logic under-voltage control signal (LOGIC). Another input of state circuit 50 receives an analog under-voltage control signal (ANALOG) and is connected to a second output of control circuit 52. An output of state circuit 50 provides a signal MODE and is connected to a control input of control circuit 52. Control circuit 52 has an input connected to bias pin 36 and another input connected to feedback pin 46 of power converter circuit 44. An output of control circuit 52 is connected to a gate of transistor 54. Both state circuit 50 and control circuit 52 are connected to ground pin 38. A drain of transistor 54 is connected to switch output pin 40 and a source is connected to ground pin 38. As those skilled in the art are aware, a gate of a transistor serves as a control terminal and the drain and source of a transistor serve as current conduction terminals. It should be noted that transistor 54 can be an insulated gate bipolar transistor (IGBT), a bipolar transistor, etc.

In operation, the line voltage, e.g., 110 VAC, is rectified by full-wave bridge rectifier 12 and filtered by capacitor 14. Secondary winding 20 provides a signal that is used to supply the operating power to electronic systems such as cable converters, computer monitors, video cassette recorders (VCRs), battery chargers, computer printers, etc. Com-

compensated error amplifier 42 provides a feedback signal to power converter circuit 44 that is proportional to the DC output signal. The output of compensated error amplifier 42 may be optically, electrically, magnetically, mechanically, or other means coupled to feedback pin 46 of power converter circuit 44.

The feedback signal is used by control circuit 52 for altering the pulse width of the signal that is supplied to the control terminal of transistor 54. Thus, compensated error amplifier 42 alters the pulse width of the output signal at switch output pin 40 in accordance with the voltage developed across terminals 26 and 28. The variable pulse width modifies the current in transformer 16, thereby regulating the voltage of the DC output signal. In addition, the bias voltage developed at bias pin 36 from secondary winding 30 can be used as the operating supply voltage of state circuit 50 and control circuit 52. The bias voltage developed at bias pin 36 can alternately be derived from secondary winding 20. It should be noted that compensated error amplifier 42 can be replaced with a high gain comparator, or the like.

FIG. 2 is a schematic diagram of state circuit 50 in accordance with the present invention. State circuit 50 includes a reference generator 60, a reset circuit 65, a positive detector circuit 76, a negative detector circuit 78, and a mode memory circuit 90. Positive detector circuit 76 and negative detector circuit 78 are referred to as a comparator circuit. In particular, reference generator 60 includes resistors 62, 64, 66, 68, 70, and 72, and a voltage clamp circuit 74. The first terminals of resistors 62 and 64 are commonly connected to state pin 48 which is connected to an input of state circuit 50. The second terminal of resistor 62 is connected to a power supply conductor which is coupled for receiving a voltage such as, for example, V_{cc} , and the second terminal of resistor 64 is connected to a power supply conductor which is coupled for receiving a reference voltage of, for example, ground. The first terminals of resistors 66 and 68 are commonly connected and form a node 67. The second terminal of resistor 66 is connected to the power supply conductor which is coupled for receiving the reference voltage of, for example, V_{cc} . The second terminal of resistor 68 and the first terminal of resistor 70 are commonly connected and form a node 69. The second terminal of resistor 70 and the first terminal of resistor 72 are commonly connected and form a node 71. The second terminal of resistor 72 is connected to a power supply conductor which is coupled for receiving a reference voltage of, for example, ground. It should be noted that the power supply conductor connected to ground is also connected to the external ground reference or ground pin 38 of power converter circuit 44 (FIG. 1). Voltage clamp circuit 74 has an input connected to node 69 and an output connected to state pin 48. By way of example, voltage clamp circuit 74 is a PNP transistor 75 having a base terminal connected to the input of voltage clamp 74, an emitter terminal connected to the output of voltage clamp circuit 74, and a collector terminal connected to a potential of, for example, ground.

The resistors 62, 64, 66, 68, 70, and 72 of reference generator 60 (FIG. 2) set reference voltages that determine the logic values of the signals at the outputs of comparators 77 and 80. By way of example, resistor 62 has a value of about 160 kilohms ($K\Omega$ s), resistor 64 has a value of about 115 $K\Omega$ s, resistor 66 has a value of about 150 $K\Omega$ s, resistor 68 has a value of about 19 $K\Omega$ s, resistor 70 has a value of about 58 $K\Omega$ s, and resistor 72 has a value of about 55 $K\Omega$ s. Resistors 62 and 64 form a resistor divider network that provides a voltage of about 2.4 volts at state pin 48 when external components are not connected at that pin. It should

be further noted that resistors 66, 68, 70, and 72 form another resistor divider network that provides voltages at nodes 67 and 71 of about 2.9 volts and about 1.1 volts, respectively. The reference voltages described are for a V_{cc} of approximately 5.8 volts. It should be noted that reference generator 60 can be configured with other combinations of resistors or alternately configured with combinations of resistors and semiconductor devices.

Positive detector circuit 76 includes a comparator 77 having a non-inverting input connected to an input of positive detector circuit 76, and thus to node 67 of reference generator 60. An inverting input of comparator 77 is connected to an input of positive detector circuit 76 and thus to state pin 48 of reference generator 60. An output of comparator 77 is connected to an output of positive detector circuit 76. Negative detector circuit 78 includes a comparator 80 connected to a pulse filter 82. Comparator 80 has a non-inverting input connected to an input of negative detector circuit 78 and thus to node 71 of reference generator 60. An inverting input of comparator 80 is connected to an input of negative detector circuit 78 and thus to state pin 48 of reference generator 60. An output of comparator 80 is coupled to an output of negative detector circuit 78 through pulse filter 82.

Reset circuit 65 receives an input signal LOGIC UNDER-VOLTAGE and has an output connected to state pin 48.

Mode memory circuit 90 includes a two-input NAND gate 84, a logic circuit 86, and a positive edge triggered toggle flip-flop 88. In particular, two-input NAND gate 84 has an input connected to the output of positive detector circuit 76, the other input is coupled for receiving the signal LOGIC UNDER-VOLTAGE. When the voltage V_{cc} begins to ramp from a starting voltage of zero volts, the signal LOGIC UNDER-VOLTAGE has an initial logic zero value that is switched to a logic one value at a predetermined voltage. By way of example, the predetermined voltage is a voltage potential that is sufficiently high to allow logic circuitry to properly operate. In other words, the signal LOGIC UNDER-VOLTAGE has a logic one value when the voltage V_{cc} is sufficiently above the predetermined voltage and a logic zero value when below the predetermined voltage.

Logic circuit 86 has an input \bar{R} coupled for receiving the signal LOGIC UNDER-VOLTAGE, an input S connected to the output of negative detector circuit 78, and an enable input E coupled for receiving the signal ANALOG UNDER-VOLTAGE. The signal ANALOG UNDER-VOLTAGE has a logic one value when the voltage V_{cc} is sufficiently high for transistors (not shown) such as, for example, the transistors in comparators 77 and 80, to operate in an analog mode. When the voltage V_{cc} is not high enough for transistors to operate in the analog mode the signal ANALOG UNDER-VOLTAGE has a logic zero value.

It should be noted that when a signal having a logic zero value is received at the input \bar{R} of logic circuit 86, the output signal at output Q of logic circuit 86 has a logic zero value. It should be further noted that when a signal having a logic one value is received at the input S of logic circuit 86, the output signal at output Q of logic circuit 86 has a logic one value. Should logic circuit 86 receive both a signal having a logic zero value at the input \bar{R} and a signal having a logic one value at the input S, the circuit responds to the signal received at the input \bar{R} . In other words, when both a set and a reset occur together, the reset function has precedence. It should be noted that the output Q can only transition from a logic zero value to a logic one value when the enable input, i.e., the signal ANALOG UNDER-VOLTAGE, is a logic one.

Toggle flip-flop 88 has an input S connected to the output of NAND gate 84, an input CLK connected to the output of logic circuit 86, and an output that also serves as the output of state circuit 50. It should be noted that the output signal of toggle flip-flop 88 can be set to a logic one value when the input S receives a logic one signal. Otherwise, the stored value of the output signal changes output state in response to logic transitions at input CLK, i.e., the stored value is toggled when the input CLK transitions from a logic zero value to a logic one value. It should be noted that if the signal at the input CLK transitions while the signal at input S is a logic one, then flip-flop 88 responds to a logic one signal at input S and ignores the signal at the input CLK.

In operation, the power supply conductor V_{cc} initially starts at a voltage of about zero volts and ramps to a higher voltage value, increasing in voltage to a voltage greater than 5.8 volts. As the voltage V_{cc} begins to ramp from zero volts, the signals LOGIC UNDER-VOLTAGE and ANALOG UNDER-VOLTAGE initially have logic zero values. The signal LOGIC UNDER-VOLTAGE is set to a logic one when the voltage V_{cc} exceeds about 3.5 volts. The signal ANALOG UNDER-VOLTAGE is set to a logic one value when the voltage V_{cc} exceeds about 4.8 volts.

In a first operating mode, no external components are connected to state pin 48. With the application of the line voltage, the voltage for V_{cc} increases from zero volts. The signal LOGIC UNDER-VOLTAGE has a logic zero value when the voltage V_{cc} is in the range of about 0 volts to about 3.5 volts. The logic zero value for the signal LOGIC UNDER-VOLTAGE causes both the output of logic circuit 86 to have a logic zero value and the output of toggle flip-flop 88 to have a logic one value. When the signal LOGIC UNDER-VOLTAGE is at a logic zero value, input state pin 48 is pulled to ground through reset circuit 65. When the voltage V_{cc} increases above a voltage of about 3.5 volts the output of reset circuit 65 becomes a high impedance output. With no external components, the voltage at state pin 48 is determined by the values of resistors 62 and 64. In this first mode of operation the voltage on state pin 48 is between the reference voltages at nodes 67 and 71, the signal at the output of comparator 77 has a logic one value, and the output of comparator 80 has a logic zero value. Thus, the signal MODE is a logic one and power supply 10 (FIG. 1) is on.

FIG. 3 is a schematic diagram of an interface switch circuit for use with the state circuit of FIG. 1 in accordance with another embodiment of the present invention. In a second operating mode, switch interface circuit 92 is connected to state circuit 50 for controlling the operation of power supply 10 (FIG. 1). Briefly referring to FIG. 3, switch interface circuit 92 includes a resistor 94, a push-button or mechanical switch 96, and a capacitor 98. In particular, a first terminal of resistor 94 is connected to a first terminal of switch 96. The second terminal of resistor 94 is connected to a power supply conductor that is coupled for receiving a voltage such as, for example, ground, and the second terminal of switch 96 is connected to a first terminal of capacitor 98, forming node 48A. Node 48A is connected to state pin 48 in this mode of operation. The second terminal of capacitor 98 is connected to a power supply conductor such as, for example, ground.

The reference voltage or reference signal at node 67 is transmitted to the non-inverting input of comparator 77 and the voltage at state pin 48 is transmitted to the inverting input of comparator 77. If the voltage at state pin 48 is less than the reference voltage at node 67, the output of comparator 77 is a logic one value. On the other hand, if the

In the second mode of operation, switch **96** allows for manually controlling whether power supply **10** (FIG. 1) is in an on-operating state or an off-operating state. Initially, the signals LOGIC UNDER-VOLTAGE and ANALOG UNDER-VOLTAGE have logic zero values. The signal LOGIC UNDER-VOLTAGE causes the output of logic circuit **86** to have a logic one value, and for state pin **48** to be grounded by reset circuit **65** and discharge capacitor **98**. The output of NAND gate **84** is a logic one value that sets the output of toggle flip-flop **88** to a logic one value.

When switch 96 is closed, capacitor 98 is discharged through switch 96 and resistor 94. The voltage at state pin 48 drops below the reference voltage at node 71 causing comparator 80 to provide a logic one to input S of logic circuit 86. The output of logic circuit 86 transitions to a logic one value causing toggle flip-flop 88 to change states such that the signal MODE is a logic one value and power supply 10 is in an on state. With each closure of switch 96 the output of logic circuit 86 transitions from a logic zero to a logic one causing the stored data in toggle flip-flop 88 to change state, provided that capacitor 98 was charged above the reference voltage at node 71.

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pin **48** and the other terminal connected to a cathode of LED **106**. An anode of LED **106** is connected to a first terminal of switch **108**. A second terminal of switch **108** is connected to a power supply conductor coupled for receiving a voltage such as, for example, V_{cc} . It should be noted that switch **108** may be a push-button switch that is closed while the button is depressed, i.e., a momentary closure.

